REMARKS

The Office Action mailed on March 30, 2001, has been received and reviewed. Claims 1-5, 11-17, 25-28, and 33-38 are currently pending in the application. Claims 1-5, 11-17, 25-28, and 33-38 stand rejected. Reconsideration of the application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Tsai discloses a method for forming shallow trench isolation structures in a semiconductor substrate. The method of Tsai includes providing a substrate that includes a silicon oxide layer thereover and a layer of silicon nitride over the silicon oxide layer. A layer of either polysilicon or silicon oxide is formed over the silicon nitride layer and acts as a sacrificial layer. A photomask that includes apertures formed therethrough at locations where trenches are to be formed in the semiconductor substrate is then formed over the sacrificial layer. Next, trenches are formed through each of the layers underlying the photomask. After the photomask has been removed, the silicon nitride layer may be descumed, or etched laterally under the overlying sacrificial layer. A thin oxide layer is then formed on the surfaces of the semiconductor substrate that are exposed within the trench. The trench is filled with a suitable dielectric material, such as tetraethylorthosilicate (TEOS). The dielectric material also forms a layer over the sacrificial layer. The dielectric material and sacrificial layer are then removed to expose the surface of the silicon nitride layer and to form an isolation structure from the dielectric material. Regions of the dielectric material that filled the descumed portion of the silicon nitride layer extend laterally beyond the outer periphery of the trench and over portions of

the silicon oxide layer. Exposed portions of the silicon oxide layer are then removed from the surface of the semiconductor substrate.

By way of contrast with the method disclosed in Tsai, independent claim 1, as presently amended and presented herein, recites a method of forming an isolation structure that includes, among other things, "selectively etching a portion of [a] buffer film layer substantially simultaneously in both horizontal and vertical directions." Amended claim 1 also recites that a layer of isolation material is applied "directly over [the] buffer film layer" and fills the trench that has been formed through the buffer film layer, an underlying dielectric layer, and into a semiconductor substrate underlying the dielectric layer.

It is respectfully submitted that neither of these elements are described, either explicitly or inherently, in Tsai. Rather, with respect to "selectively etching a portion of [the] buffer film layer *substantially simultaneously in both horizontal and vertical directions*" (emphasis supplied), Tsai illustrates, in FIG. 3D, and discloses removal of material of the sacrificial layer, the silicon nitride layer, the silicon oxide layer, and portions of the underlying semiconductor substrate in only a vertical direction. Contrary to the assertion in the fourth paragraph of page 2 of the outstanding Office Action, Tsai does not explicitly or inherently describe isotropic etching of the silicon nitride layer. Rather, Tsai, at col. 3, lines 5-8, merely discloses "....a shallow trench 38 is formed by etching portions of the sacrificial layer 36, the silicon nitride layer 34, pad oxide 32 and the substrate 30...". Tsai then discloses, at col. 3, lines 19-28, that portions of the silicon nitride layer may subsequently be descumed, undercutting the silicon nitride layer about 50-1,000Å beneath the overlying sacrificial layer. Thus, Tsai does not disclose that the silicon nitride layer may be etched substantially simultaneously in both horizontal and vertical directions as set forth in presently amended independent claim 1.

In further contrast is the presently claimed invention of independent claim 1, with respect to the application of a layer of isolation material *directly over* the buffer film layer, Tsai merely discloses that the dielectric material that fills the trench may contact edges of the silicon nitride layer formed between the sacrificial layer and the silicon oxide layer by the descuming process.

Accordingly, Tsai does not explicitly or inherently describe "applying a layer of isolation material directly over" the silicon nitride layer.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 102(e), amended claim 1 is allowable over Tsai.

Claims 2-4 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Independent claim 11, as presently amended and presented herein, recites, among other things, "selectively etching a portion of [the] buffer film layer substantially simultaneously in both horizontal and vertical directions" and "applying a layer of isolation material directly over [the] buffer film layer..." As Tsai lacks any explicit or inherent description regarding both of these elements, it is respectfully submitted that, under 35 U.S.C. § 102(e), amended claim 11 is allowable over Tsai.

Claims 12-14 and 16 are each allowable, among other reasons, as depending either directly or indirectly from claim 11, which is allowable.

The method of independent claim 25, as presently amended and presented herein, also includes, among other things, "selectively etching a portion of [a] buffer film layer substantially simultaneously in both horizontal and vertical directions, " as well as "applying a layer of isolation material directly over [the] buffer film layer...." Again, Tsai does not explicitly or inherently describe either of these elements of the presently claimed invention. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 25 is allowable over Tsai.

Both claims 26 and 27 depend from claim 25, which is allowable. Therefore, both claims 26 and 27 should also be allowed.

Independent claim 33, as presently amended and presented herein, recites a method that includes, among other things, "selectively etching a portion of [a] buffer film layer substantially simultaneously in both horizontal and vertical directions" and "applying a layer of isolation material directly over [the] buffer film layer..." Tsai does not explicitly or inherently describe that the silicon nitride layer thereof, an exemplary buffer film layer, may be substantially

simultaneously etched in both horizontal and vertical directions. Nor does Tsai explicitly or inherently describe that a layer of isolation material may be applied directly over a buffer film layer. Thus, it is respectfully submitted that Tsai does not explicitly or inherently describe each and every element of amended claim 33 and that amended claim 33 is, therefore, allowable under 35 U.S.C. § 102(e).

Each of claims 34, 35, and 37 is allowable, among other reasons, as depending either directly or indirectly from claim 33, which is allowable.

In view of the foregoing, it is respectfully requested that Office withdraw the 35 U.S.C. § 102(e) rejections of claims 1-4, 11-14, 16, 25-27, 33-35, and 37.

Rejections Under 35 U.S.C. § 103(a)

Tsai in View of Pan

Claims 5, 15, 28, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai, as applied to claims 1-4, 11-14, 16, 25-27, 33-35, and 37 above, and further in view of U.S. Patent 5,834,358 to Pan et al. (hereinafter "Pan"). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Since Pan issued from an application that was filed before the earliest priority date to which the above-referenced application is entitled, but did not issue until after the earliest priority date for the above-referenced application, Pan qualifies as prior art under 35 U.S.C. § 102(e). As Micron Technology, Inc., is the assignee of Pan and since the above-

referenced application is also assigned to Micron Technology, Inc., it is respectfully submitted that 35 U.S.C. § 103(c) prevents the use of Pan in a 35 U.S.C. § 103(a) rejection of any of the claims of the above-referenced application. Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of claims 5, 15, 28, and 36 is respectfully requested.

Further, each of claims 5, 15, 28, and 36 is allowable, among other reasons, as respectively depending from claims 1, 11, 25, and 33, each of which is allowable for the reasons previously provided herein.

Tsai in View of the Examiner's Comments

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai as applied to claims 1-4, 11-14, 16, 25-27, 33-35, and 37 above, and further in view of the Examiner's comments.

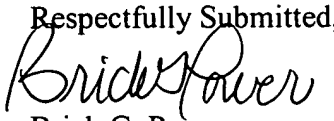
Claim 17 is allowable, among other reasons, as depending from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, as depending from claim 33, which is allowable.

CONCLUSION

Claims 1-5, 11-17, 25-28, and 33-38 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should it be determined that additional issues remain which might be resolved by a telephone conference, the Office is respectfully invited to contact the undersigned attorney.

Respectfully Submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Three times amended) A method of forming an isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions;

applying a layer of isolation material directly [to] over said buffer film layer and filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

11. (Three times amended) A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions to expose opposing trench edges at an intersection of said trench sidewalls and an upper surface of said semiconductor substrate;

applying a layer of isolation material directly [to] over said buffer film layer and filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

25. (Four times amended) A method of forming an isolation structure on a semiconductor device layered structure [including] that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, [wherein] an oxide layer [is formed] being located on [exposed] portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions;

applying a layer of isolation material directly [to] over said buffer film layer and filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

33. (Three times amended) A method of forming a capped shallow trench isolation structure for a semiconductor device layered structure [including] that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and extending into said semiconductor substrate, [wherein] an oxide layer [is formed] being located on [exposed] portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material directly [to] over said buffer film layer and filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.